

# VCSEL arrays for high aggregate bandwidth of up to 1.34 Tbps

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## Abstract

Even though the lane speed of VCSEL based AOC and transceivers has reached 25 Gbps and beyond [1-7], parallel optics are getting even more important in order to meet the increasing demand for aggregate bandwidths in upcoming applications, among others, 100 Gigabit Ethernet, Infiniband EDR, or EOM (embedded optical modules). As 100 Gbps can be achieved by, e.g., 4 times 25 Gbps using standard QSFP form factor, different approaches are using large scale 2D VCSEL arrays operating at lower lane speeds. Early work on 2D VCSEL based transceivers has already been presented beginning of this century [8] and recent work also addressed the potential of this technology [9,10]. In 2013, Compass EOS has introduced a 1.34 Tbps core router solution [11,12,13] that incorporates 2D VCSEL arrays of 14x12 emitters designed and manufactured by Philips U-L-M Photonics. The VCSEL array is mounted face down onto a CMOS ASIC, directly on top of the analog area. The emission wavelength of 1000 nm allows for substrate side emission and thus for flip-chip mounting as well as the possibility of integrating 2D microlens arrays onto the stack of CMOS and VCSEL array.

After briefly introducing the router with regard to the incorporated VCSEL technology we discuss the design and performance of the VCSEL array. Finally, the assembly solution for this most compact and dense transceiver solution is presented.

**Keywords:** VCSEL, VCSEL array, EOM, flip-chip, chip-on-chip

## Introduction

Within routers, data distribution between line cards has been identified as one main bottleneck for performance. In 2013 Compass EOS introduced the r10004 Router which incorporates an optical transceiver solution based on 12x14 channels and according fiber management for data distribution between line cards as well as racks [11]. The full duplex 1.34 Tbps transceivers provide 64 Gbps/mm<sup>2</sup> data density. Fig. 1 shows the compactness of the r10004 Router which also provides very low power consumption of only 10.2 pF/bit, incl. SERDES on smallest footprint. The transceiver is monolithically built into the CMOS ASIC by monolithic analog & digital ASIC design, and the VCSEL and PD arrays are flip-chip mounted onto the analog part of the ASIC [13]. The subassembly is then flip-chipped onto a substrate carrying the ball grid array (BGA) that allows for on board system integration. In Fig 2. the two step flip-chip assembled optical module is presented, revealing the optical interfaces of VCSEL and PD arrays in the

center of the BGA. As a subsequent step microlens arrays are placed onto the VCSEL and PD arrays for fiber coupling.



**Fig. 1:** Compass-EOS r10004 Router. Optical chip-to-chip data distribution by using 2D VCSEL and PD arrays flip-chipped on ASIC.

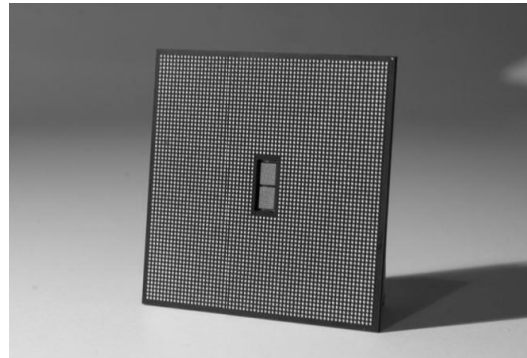


**Fig. 2:** 2D VCSEL and PD arrays (center) flip-chipped on CMOS ASIC and subsequently flip-chipped on a substrate with BGA, representing a 1.34 Tbps optical transceiver.

### Design of large scale 2D bottom emitter array

Stacking of optical chips onto CMOS requires advanced assembly technology and a different device design for VCSELs and PDs compared to today's standard array formats. Due to the necessity of flip-chip bonding instead of wire bonding for 2D arrays, bottom-emission is required which can be enabled by either longer wavelength above the fundamental absorption of GaAs or substrate removal technologies [8]. The extremely compact design of stacked 2D VCSEL arrays on CMOS and the elevated temperature by self-heating of the CMOS itself, results in challenging thermal boundary conditions. The requirements for VCSEL arrays are low power consumption, good high speed performance, excellent heat removal, and sufficient mechanical robustness in order to withstand the advanced assembly procedures. Oxide confined VCSELs emitting at 1000 nm wavelength have been chosen, as they are based on mature DBR designs while the GaAs substrate is already transparent and can act as mechanical base as well as heat distributing layer.

Fig. 3 shows a cross section of the VCSEL design. The Quantum Wells are built of InGaAs with GaAs as barriers. The dry etched mesa is covered by a full size p-contact, the p-electrode pad is placed on 3  $\mu\text{m}$  polyimide passivation layer. The cathode pad is elevated by electroplated Au pillars to the same level as the p-electrode pad. For improved thermal management additional pads are thermally connected by electroplated Au-pillars to the substrate, but electrically isolated by dielectric barriers.

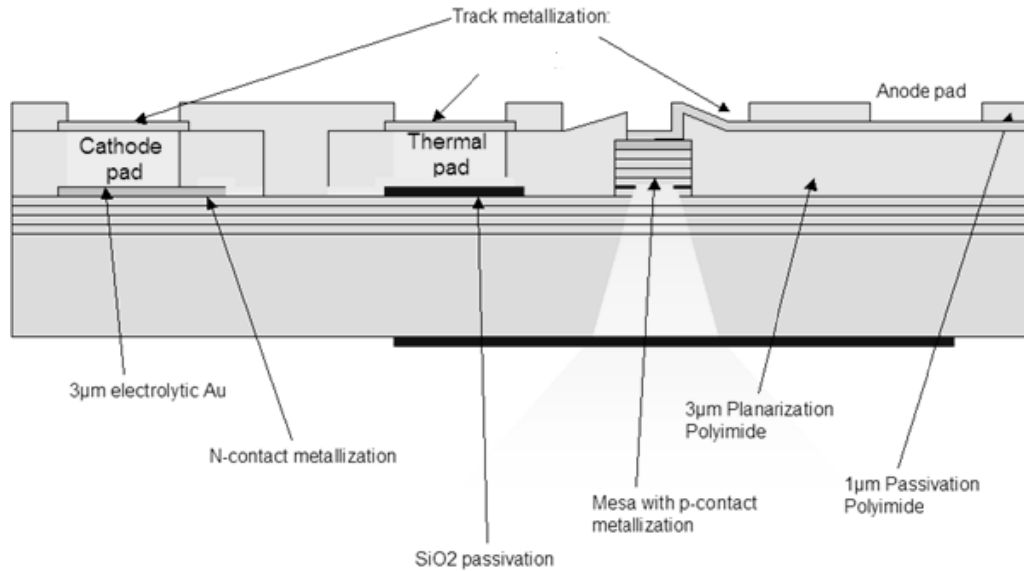


**Fig. 3: Design of the 1000 nm bottom-emitting VCSEL. The active layers are built of InGaAs/GaAs QWs and the current confinement is controlled by selective oxidation. Electroplated Au pillars provide improved heat flow to the solder interface. The substrate back side is AR coated with dielectric single layer.**

Efficient current confinement to an 8 micron aperture just above the active region is achieved by an oxide layer, which in combination with small mesa geometries and according low parasitics results in high performance of the device. The substrate is AR coated with a single dielectric layer. As the VCSEL arrays are designed for flip-chip soldering using eutectic AuSn depots, non-wettable cover layers built of an additional Polyimide layer protect the chip surface against creeping of solder along the metal tracks.

The channel to channel pitch of 250  $\mu\text{m}$  is matching the geometries of standard fiber bundles and thus the VCSEL array dimensions result in 3.5 x 3.0 mm<sup>2</sup>.

### **CW performance of 1000 nm bottom emitters**

A fundamental requirement for large scale 2D VCSEL arrays is an excellent parametric uniformity of the performance parameters and of course a very high yield on wafer level that enables a reasonable yield on array level. Fig. 4 depicts the room temperature LIV characteristics of 168 VCSELs arranged in a 14x12 matrix. The curves are practically identical, showing a threshold current of 0.5 mA and an operating voltage and output power of 1.9 V and 1.9 mW, respectively, at 6.0 mA laser current.

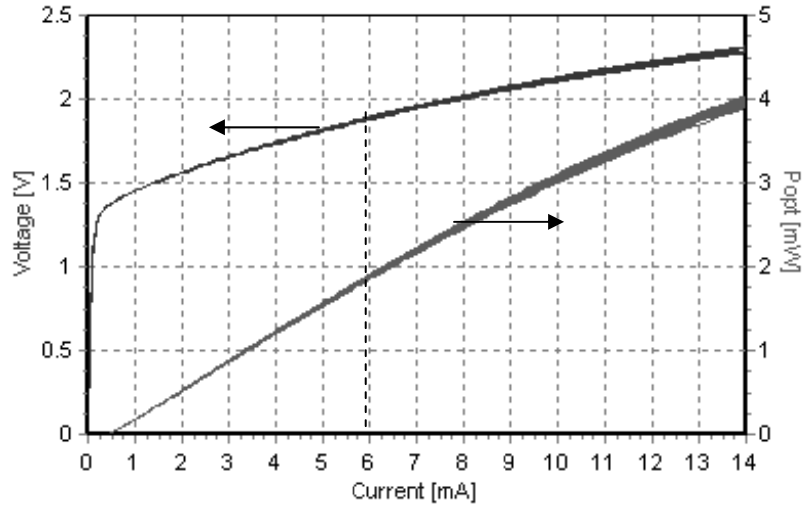


**Fig. 4: CW LIV performance of the 1000 nm bottom-emitting VCSEL array. 168 channels are plotted in the diagram and show excellent homogeneity. At operating bias current of 6.0 mA the respective voltage drop is only 1.9 V.**

Analyzing the distribution of parameters across an entire production wafer, very narrow distributions of parameters can be noticed. In Fig. 5 the mean value for all 38.304 channels on wafer (no upfront selection of in-spec VCSELs) is given as 0.503 mA, with an according standard deviation of only 0.037 mA. For the slope efficiency, values are shown in Fig. 6, the mean value is calculated to 0.342 W/A, the standard deviation 0.013 W/A.

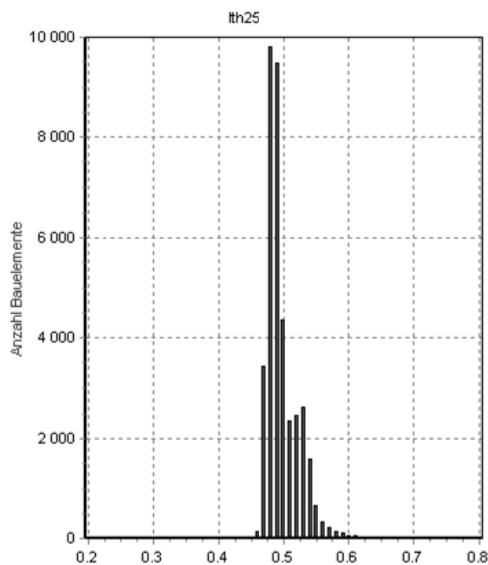


**Fig. 5: Threshold current distribution across a full wafer. Mean value results in 0.503 mA and the standard deviation is 0.037 mA.**

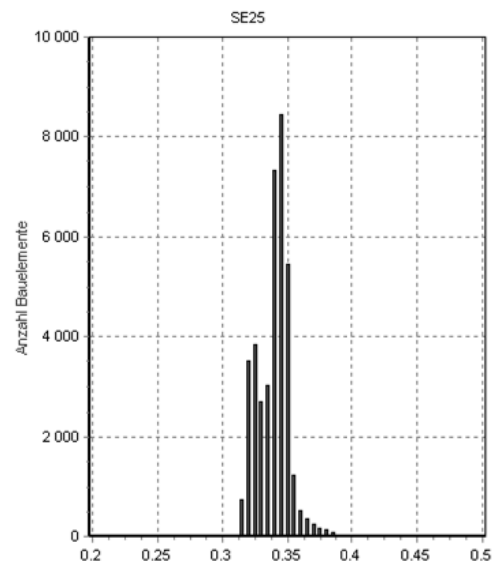


**Fig. 6: Slope efficiency distribution across a full wafer. Mean value results in 0.342 W/A and the standard deviation is 0.013 W/A.**

Also for the differential resistance the distribution is very narrow. Mean value is 70.0 Ohm and the standard deviation is 5.0 Ohm. The parametric uniformity is excellent and the according on wafer channel yield has been demonstrated as high as 98.9%. Such homogeneity can only be achieved by superior control of epitaxial growth and oxide apertures.

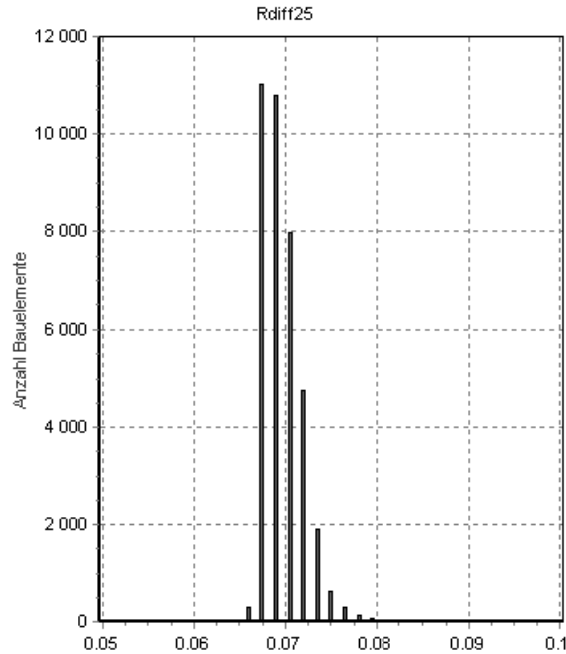


**Fig. 7: Slope efficiency distribution across a full wafer. Mean value results in 70.0 Ohm and the standard deviation is 5.0 Ohm.**

In addition to the VCSEL performance requirements, another challenge is the on wafer measurement of the VCSEL parameters itself. Whilst both electrodes, anode and cathode, are accessible from the top side, the emitted power can only be measured at the backside of the wafer. Therefore the wafer chuck of the wafer probing station must be either transparent or needs to allow for free standing substrate during the probing. The latter solution does enable a measurement without potentially disturbing optical interfaces and respective fringes. The remaining substrate thickness of 500  $\mu\text{m}$  does support the measurements mechanically. The wafer thus can be mapped identically to top-emitting VCSEL wafers, but with the optical power meter beneath the substrate.

### **High frequency performance of 1000nm bottom emitters**

The large signal performance of the bottom-emitting VCSEL at room temperature is presented in Fig. 8, showing an eye diagram measured for a bit sequence of PRBS  $2^{31}-1$ . The unmounted

VCSEL is operated at 6.0 mA average laser current and 5.5 mA modulation current by using a high speed probe. The resulting mask margin is calculated to 30%. The corresponding rise and fall times extracted from the curves given in Fig. 9 are 31 ps and 50 ps, respectively. The introduced VCSEL design does provide satisfactory margin for the targeted data rate.

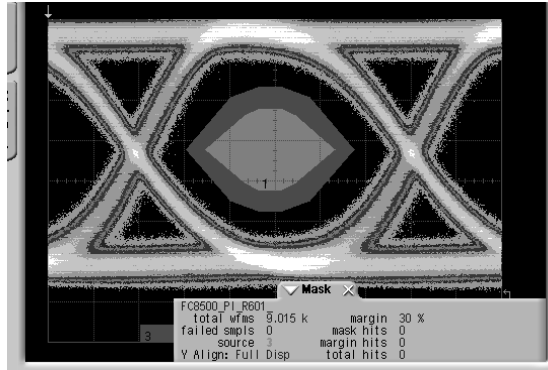


**Fig. 8: Eye diagram measured with high speed probe on a unmounted channel at room temperature. At a data rate of 8 Gbps 30% mask margin is achieved.**

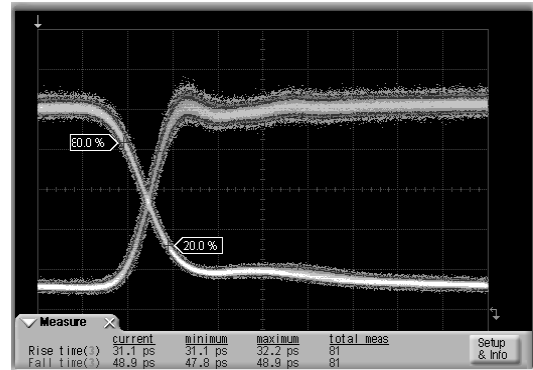


**Fig. 9: Measurement results for rise and fall time results in 31 ps and 50 ps, respectively.**

The uniformity of the high speed performance within an array can be seen from the 14x12 arrangement of eye diagrams in Fig. 10. The eye diagrams have been measured sequentially at identical operating conditions of 6.0 mA average current and 5.5 mA modulation current. All 168 eye diagrams are wide open and rather comparable.

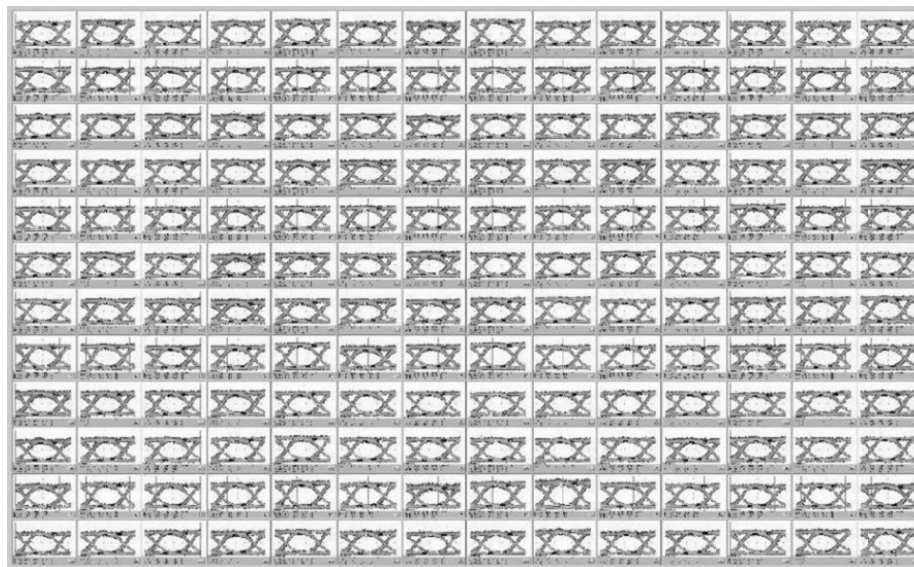


**Fig. 10: Eye diagrams for all 168 channels in a large scale 2D VCSEL array, measured at room temperature, 8 Gbps with PRBS  $2^{31}-1$  sequence, and 6 mA bias current.**

More meaningful than eye diagrams measured by using pattern generator and high speed probes are the results obtained from fully assembled optical engines or transceivers. Fig. 11 shows the eye diagram of one channel within a fully assembled VCSEL array, mounted flip-chip onto and driven by the CMOS ASIC. Due to the elevated VCSEL chip temperature of 65°C caused by the self-heating from the ASIC, the average laser current has been set a bit higher to 6.5 mA in order to address the slightly increased threshold current. The modulation current again is set to 5.5 mA.

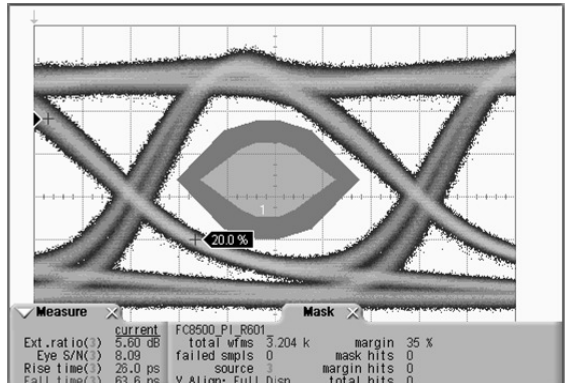


**Fig. 11: Eye diagram of a flip-chip mounted 1000 nm bottom-emitting VCSEL operated at 6.5 mA bias and 65°C chip temperature. Mask margin is 35%.**

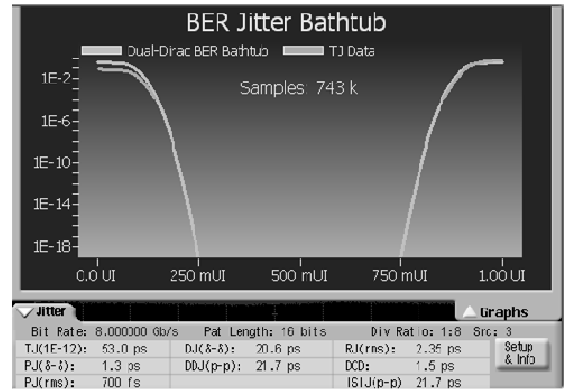


**Fig. 12: BER rate measurements result in total Jitter of 0.5 UI at BER  $10^{-18}$ .**

The resulting eye diagram again is wide open and provides an excellent mask margin of 35%. Measurements of Bit Error Rates (BER) and according extrapolations show a total Jitter of 0.5 UI for BER down to  $10^{-18}$ .

### System integration of 1000 nm bottom emitting VCSEL array

Compared to the standard assembly technology of today's QSFP or CXP optical engines, where typically die attach by epoxy glue and wire bonding is still state of the art, the flip-chip assembly of large scale VCSEL arrays is very special and demanding. The necessity of sequential soldering steps requires a high temperature solder for the first flip-chip process. Eutectic AuSn pillars are used for the VCSEL/ASIC interface. Non-wettable areas on the VCSEL top surface avoid creeping of AuSn along the metal tracks towards critical areas. AuSn bumps and an optical die soldered onto the ASIC can be seen in Fig. 13.

A fully assembled ASIC with VCSEL and PD die soldered by flip-chip onto the analog area of the ASIC is shown in Fig. 14. In total 672 electrically functional joints as well as many more thermal joints are established for this optical subassembly. The area used for the optical transceiver is covering only about 10% of the total ASIC area.

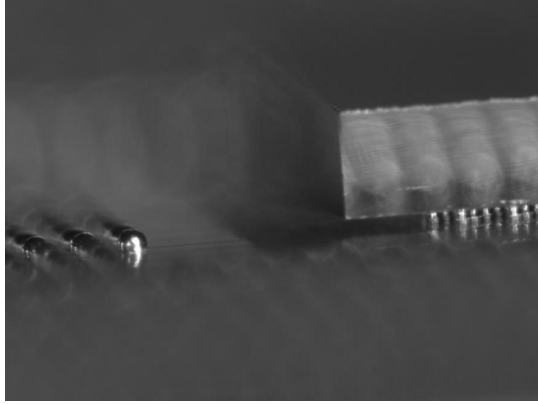


**Fig. 13: AuSn bumps are used for flip-chipping the VCSEL array onto the CMOS ASIC.**

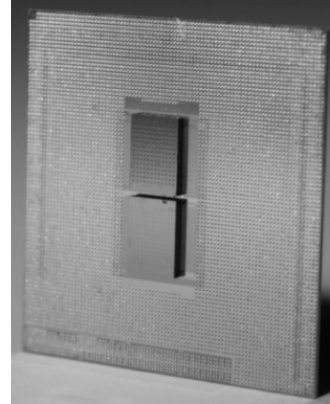


**Fig. 14: Both, VCSEL and PD arrays placed on the CMOS ASIC by flip-chip technology. The transceiver area consumes about 10% of the total ASIC area.**

The optical subassembly is then soldered to a substrate carrying the BGA (see Fig. 2) and finally mounted to the backside of the system board. On the opposite side of the system board, the fiber bundle is aligned and fixed to the optical subassembly, as shown in Fig. 15. The final transceiver is capable of carrying 1.34 Tbps full duplex. Such high density optical systems can only be realized based on VCSEL technology which intrinsically enables 2D arrangements ideally matching CMOS technology.

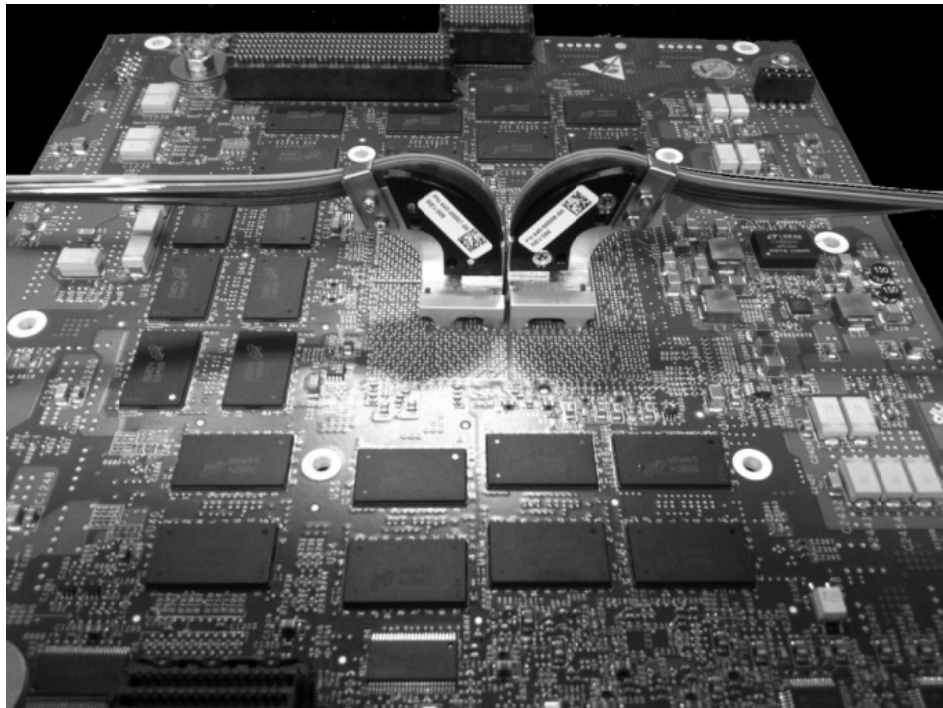


**Fig. 15: 1.34 Tbps optical transceiver assembled onto the system board.**

## Conclusion

The r10004 Router released by Compass-EOS is making use of a primary VCSEL technology promise: the stacking of ASIC and 2D VCSEL array together with micro lens arrays for 2D fiber coupling that results in a most compact optical transceiver. The further demand for higher aggregate bandwidth will have to be addressed by increasing lane speeds even beyond 25 Gbps, but upscaling in orders of magnitude will only be possible by highly parallel solutions. Both directions need to be further enhanced simultaneously. Combining already demonstrated building blocks, like 28 Gbps single lane data rates and the presented assembly solution, the aggregate bandwidth already provides the capability to reach 4.7 Tbps.

## Aknowledgements

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## References

- [1] D. M. Kuchta et al., "A 55Gb/s Directly Modulated 850nm VCSEL-Based Optical Link", IEEE Photonics Conference 2012 (IPC 2012) Post Deadline Paper PD 1.5 (2012).
- [2] S.A. Blokhin et al., "850 nm VCSELs operating at bit rates up to 40 Gbit/s", Electronics Letters 45, pp. 501-503 (2009).
- [3] Toshihito Suzuki et al., "Reliability study of 1060 nm 25 Gbps VCSEL in terms of high speed modulation", Proc. SPIE 8276, pp. 04-01 to 04-8 (2012).
- [4] AVAGO Technologies, [http://www.avagotech.com/pages/video\\_ofc2011\\_25g\\_vcsel](http://www.avagotech.com/pages/video_ofc2011_25g_vcsel) (2011).
- [5] Neinyi Li et al., "Emcore's 1 Gb/s to 25 Gb/s VCSELs", Proc. SPIE vol. 8276, pp. 03-1 to 03-10 (2012).
- [6] M. Grabherr et al., "25 Gbps and beyond: VCSEL development at Philips", Proc. of SPIE Vol. 8639, pp. 0J-1 to 0J12 (2013).
- [7] Afriat Gil et al., "VCSEL based optical transceiver module operating at 25 Gb/s and using a single CMOS IC", Proc. of SPIE Vol. 8282, paper 06, pp. 1-6 (2012).
- [8] M. Grabherr et al., "Comparison of approaches to 850 nm 2-D VCSEL arrays", Proc. of SPIE Vol. 4994, pp. 83-91 (2003).
- [9] Clint L. Schow et al., "A 24-Channel, 300 Gb/s, 8.2 pJ/bit, Full-Duplex Fiber-Coupled Optical Transceiver Module Based on a Single "Holey" CMOS IC," J. Lightwave Technol. **29**, 542-553 (2011).
- [10] Pinxiang Duan et al., "A novel 3D stacking method for Opto-electronic dies on CMOS ICs," Opt. Express **20**, B386-B392 (2012)

- [11] Kobi Hasharoni et al., “A high end routing platform for core and edge applications based on chip to chip optical interconnect”, OTu3H.2, OFC/NFOFC (2013).
- [12] S. Benjamin et al., “Assembly of 1.3 Tb/s Full Duplex Optical Module“, Proc. IEEE 63<sup>rd</sup> Electronic Components and Technology Conference (ECTC), pp. 292-296 (2013).
- [13] Kobi Hasharoni et al., “A 1.3 Tb/s parallel optics VCSEL link”, Proc. SPIE vol. 8991, paper 10 (2014).